



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Art Unit 2154 Examiner Larry Donaghue

In Re: Stephen Melvin et al.
Case: P3813
Serial No.: 09/592,106
Filed: 06/12/2000
Subject: Method and Apparatus for Implementing Atomicity of Memory Operations in Dynamic Multi-Streaming Processors

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Information Disclosure Statement under 37 C.F.R. §1.97

Enclosed herewith is an Information Disclosure Statement (IDS) by Applicant listing fifty-five (55) references. Under §1.98(d) no reference copies are required as they have been provided in priority application s/n 09/737,375. Applicant desires that the references be entered in the above-mentioned case as relevance dictates.

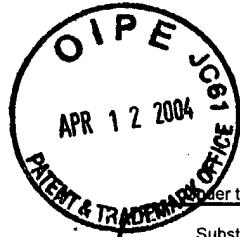
As this IDS is being filed with an RCE, in accordance with rule 1.97(b)(3), no additional fee is required. Please charge any deficiency or credit any overpayment to Deposit Account No. 50-0534.

Respectfully submitted,
Stephen Melvin et al.
by


Donald R. Boys
Reg. No. 35,074

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(831) 726-1457

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Application Number	09/592,106
Filing Date	06/12/2000
First Named Inventor	Stephen Melvin
Art Unit	2154
Examiner Name	Larry D. Donaghue
Attorney Docket Number	P3813

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Attorney Docket Number P3813

U. S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
		US- 5600837 A *	02-04-1997	Artieri, Alain	
		US- 5461722 A *	10-24-1995	Goto, Tatuhiro	
		US- 5542088 A *	07-30-1996	Jennings, Jr. et al.	
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		Number-Kind Code ² (if known)			
		US- 6535905 B1 *	03-18-2003	Kalafatis et al.	
		US- 4200927 A *	04-29-1998	Hughes et al.	
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		US- 5815733 A *	09-29-1998	Anderson et al.	Technology Center 2100
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		* FISKE et al., "Thread Prioritization: A Thread Scheduling Mechanism for Multiple-Context Parallel Processors", 1995, pp 210 -221, IEEE	
		* YAMAMOTO, Wayne, "An Analysis of Multistreamed, Superscalar Processor Architectures", University of California Santa Barbara dissertation, December 1995, Santa Barbara, US	
		* STEERE et al., "A Feedback - Driven Proportion Allocator for Real-Rate Scheduling", Third Symposium on Operating Systems Design and Implementation, February 1999, pp 145-158, USENIX Association	
		* YAMAMOTO et al., "Increasing Superscalar Performance Through Multistreaming", 1995	
		* TULLSEN et al., "Simultaneous Multithreading: Maximizing on-Chip Parallelism", 22nd Annual International Symposium on Computer Architecture, June 1995, Santa Margherita Ligure, Italy	
		* YOAZ et al., "Speculation Techniques for Improving Load Related Instruction Scheduling", 1999, pp 42-53, IEEE	
		* KESSLER, R.E., "The Alpha 21264 Microprocessor: Out-of-Order Execution at 600 Mhz", August 1998	
		* YAMAMOTO ET AL., Performance Estimation of Multistreamed, Superscalar Processors, IEEE. 1994, pp 195-204, Hawaii, US	
		* NEMIROVSKY et al., "Quantitative Study of Data Caches on a Multistreamed Architecture", Workshop on Multithreaded Execution Architecture and Compilation, January 1998	
		* LI et al., "Design and Implementation of a Multiple-Instruction-Stream Multiple-Execution-Pipeline Architecture", 7th International Conference on Parallel and Distributed Computing and Systems, October 1995, Washington D.C.	

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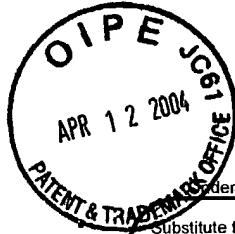
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		* The PowerPC Architecture: A Specification for a New Family of RISC Processors, Second Edition, May 1994, pp 70-72, Morgan Kaufmann, San Francisco	
		* MC68020 32-Bit Microprocessor User's Manual, Third Edition, 1989, pp 3-125, 3-126, and 3-127, Prentice Hall, New Jersey	
		* POTEL, M.J., Real-Time Playback in Animation Systems, Proceedings of the 4th Annual Conference on Computer Graphics and Interactive Techniques, 1977, pp. 72-77, San Jose, CA	
		* ARM Architecture Reference Manual, 1996, pp. 3-41, 3-42, 3-43, 3-67, 3-68, Prentice Hall	
		* ESA/390 Principles of Operation, IBM Library Server, 1993 , Table of Contents and Para. 7.5.31 and 7.5.70 (available at : http://publibz.boulder.ibm.com/cgi-bin/bookmgr_OS390/BOOK/DZ9AR001/CCONTENTS)	
		* MC88110 Second Generation RISC Microprocessor User's Manual, 1991, pp. 10-66, 10-67 and 10-71, Motorola, Inc.	
		* DIEFENDORFF, KEITH et al., Organization of the Motorola 88110 Superscalar RISC Microprocessor, IEEE Micro, April 1992, pp.40-63, Vol. 12, No. 2	
		* KANE, GERRY, PA-RISC 2.0 Architecture, 1996, pp 7-106 and 7-107, Prentice Hall, New Jersey	
		* DIEFENDORFF, KEITH et al., AltiVec Extension to PowerPC Accelerates Media Processing, March - April 2000, pp. 85-95, IEEE Micro, Vol. 20, No. 2	
		* NEMIROVSKY ET AL., DISC: Dynamic Instruction Stream Computer, ACM, 1991, pp 163-171	

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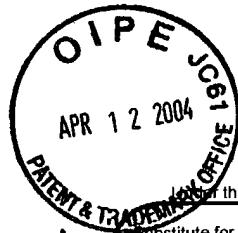
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First Named Inventor: **Stephen Melvin**

Serial Number: **09/592,106**

Filing Date: **06/12/2000**

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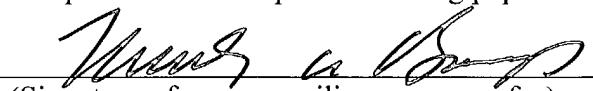
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